

Refine Search

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L4 and L5	2

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L26

Refine Search

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Search History

DATE: Thursday, October 28, 2004 [Printable Copy](#) [Create Case](#)

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 result set

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

<u>L26</u>	l4 and l5	2	<u>L26</u>
<u>L25</u>	L23 and l12	3	<u>L25</u>
<u>L24</u>	L23 and l20	6	<u>L24</u>
<u>L23</u>	714/\$.ccls.	46830	<u>L23</u>
<u>L22</u>	l20 and L13	12	<u>L22</u>
<u>L21</u>	buffer\$1 same L13	2367	<u>L21</u>
<u>L20</u>	buffer\$1 and L19	57	<u>L20</u>
<u>L19</u>	(dram module\$1) and dimm	115	<u>L19</u>
<u>L18</u>	(dram module\$1) and l17	0	<u>L18</u>
<u>L17</u>	(signal path\$1) same (edge connector\$1)	85	<u>L17</u>
<u>L16</u>	L13 and l12	8	<u>L16</u>
<u>L15</u>	L14 and l12	1	<u>L15</u>
<u>L14</u>	test\$5 near4 dram\$1	2490	<u>L14</u>
<u>L13</u>	test\$5 near4 memory	35456	<u>L13</u>

<u>L12</u>	(map\$5 near4 pin\$1) same buffer\$1	37	<u>L12</u>
<u>L11</u>	L9 and l1	4	<u>L11</u>
<u>L10</u>	L9 and l4	0	<u>L10</u>
<u>L9</u>	(switching circuit\$1) and (test\$5 near3 dram\$1)	186	<u>L9</u>
<u>L8</u>	(bypass\$5 near3 buffer\$1) and l5	0	<u>L8</u>
<u>L7</u>	(differential signal\$1) and l5	0	<u>L7</u>
<u>L6</u>	(differential signal\$1) and l4	2	<u>L6</u>
<u>L5</u>	test\$5 near3 (dram module\$1)	20	<u>L5</u>
<u>L4</u>	coupl\$5 near4 (dram module\$1)	64	<u>L4</u>
<u>L3</u>	(dimm\$1 same tester\$1) same buffer\$1	5	<u>L3</u>
<u>L2</u>	(coupl\$5 near3 tester\$1) near3 buffer\$1	4	<u>L2</u>
<u>L1</u>	test\$5 same (dram near3 module\$1)	176	<u>L1</u>

END OF SEARCH HISTORY